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TYNEMOUTH SOFTWARE 68B50 SERIAL CARD WITH CLOCK FOR RC2014

PARTS LIST

CAPACITORS – CERAMIC RATED 6.3V OR HIGHER

2 x 18-22pF axial (to suit crystal) *(usually marked 18p/20p/22p or 180/200/220)*
1 x 100nF axial *(usually marked 100n or 104)*

RESISTORS – ALL ¼W 5% OR BETTER (4 BAND RESISTOR COLOUR CODES SHOWN)

3 x 1KΩ
3 x 2.2KΩ
1 x 1MΩ

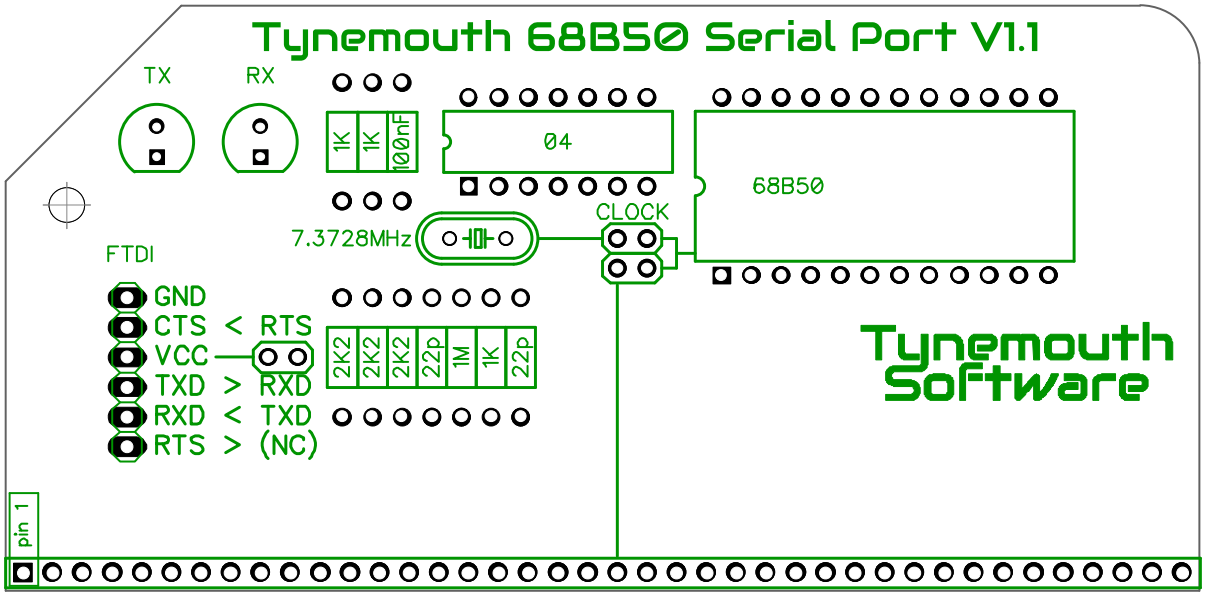
SEMICONDUCTORS

1 x 74HC04 (*alternatively LS, HCU or HCT*)
1 x 68B50 (*6850 should also work, although it would be running higher than the specified speed*)
1 x 7.3728 MHz HC49U Crystal
1 x Red 5mm LED
1 x Green 5mm LED

CONNECTORS / SWITCHES

1 x 40 way 0.1” right angled header
1 x 6 way 0.1” right angled header
3 x 0.1” 2 way header and jumpers or wire links as required

COMPONENT PLACEMENT



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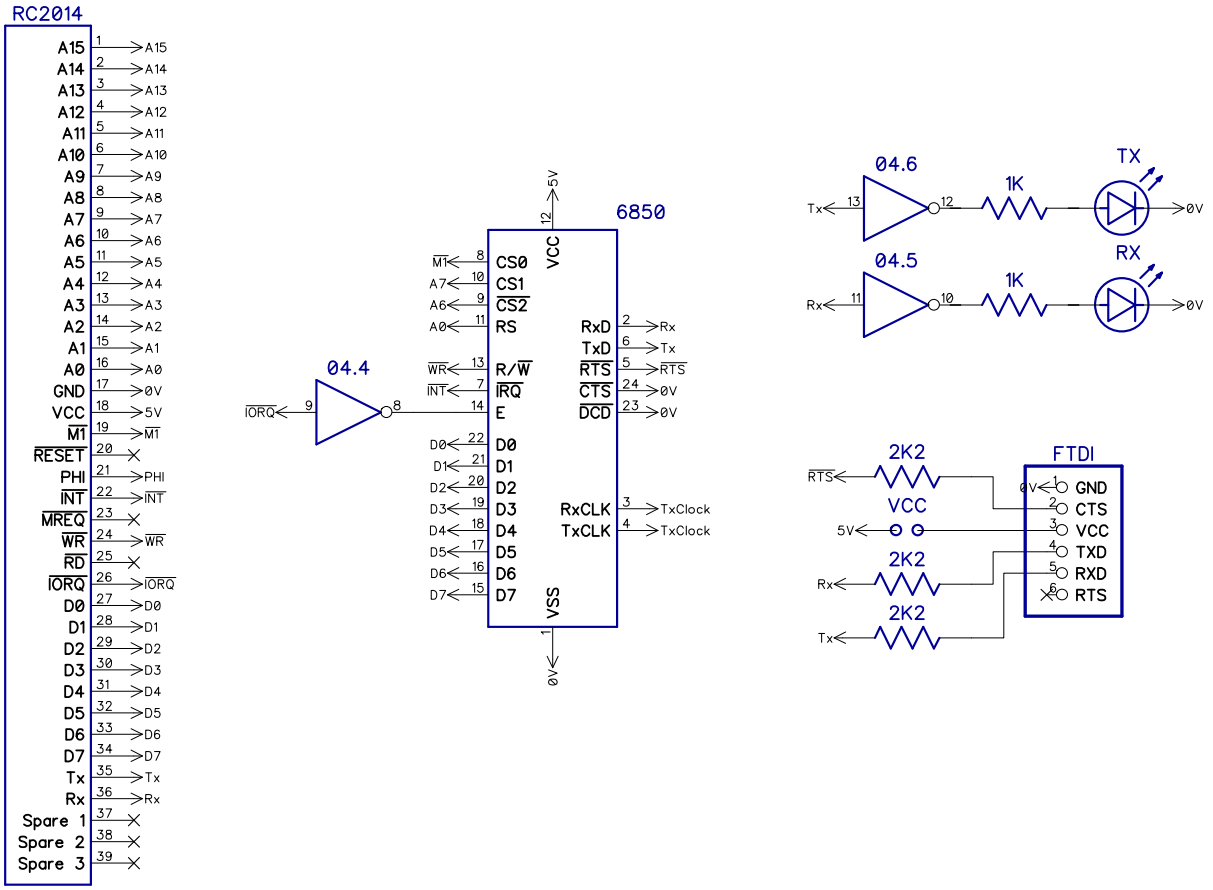
SERIAL INTERFACE

SCHEMATIC



CONNECTIONS

The 68B50 UART is interfaced to the RC2014 bus using the four chip select / enable lines on the 68B50 for address decoding. The device is active when /M1 and A7 are high, and A6 and /IORQ are low (/IORQ being inverted to achieve this). This decodes as an IO request to an address from 0x80 to 0xBF. A0 is used to select the two register inside the 6850.

The serial Rx, Tx and RTS are connected to the FTDI connector via 2K2 resistors to protect from shorts.

5V from the FTDI connector can be jumpered to power the rest of the RC2014 system.

The Rx and Tx lines are buffered by two spare inverters to drive LEDs which flash with activity (single character pulses are quite short, so the flashes are brief unless multiple characters are being sent or received).

The Tx and Rx clock is provided by the clock circuit.

The interrupt line /INT is connected to the 68B50 and can be triggered on errors, data transmitted and data received.

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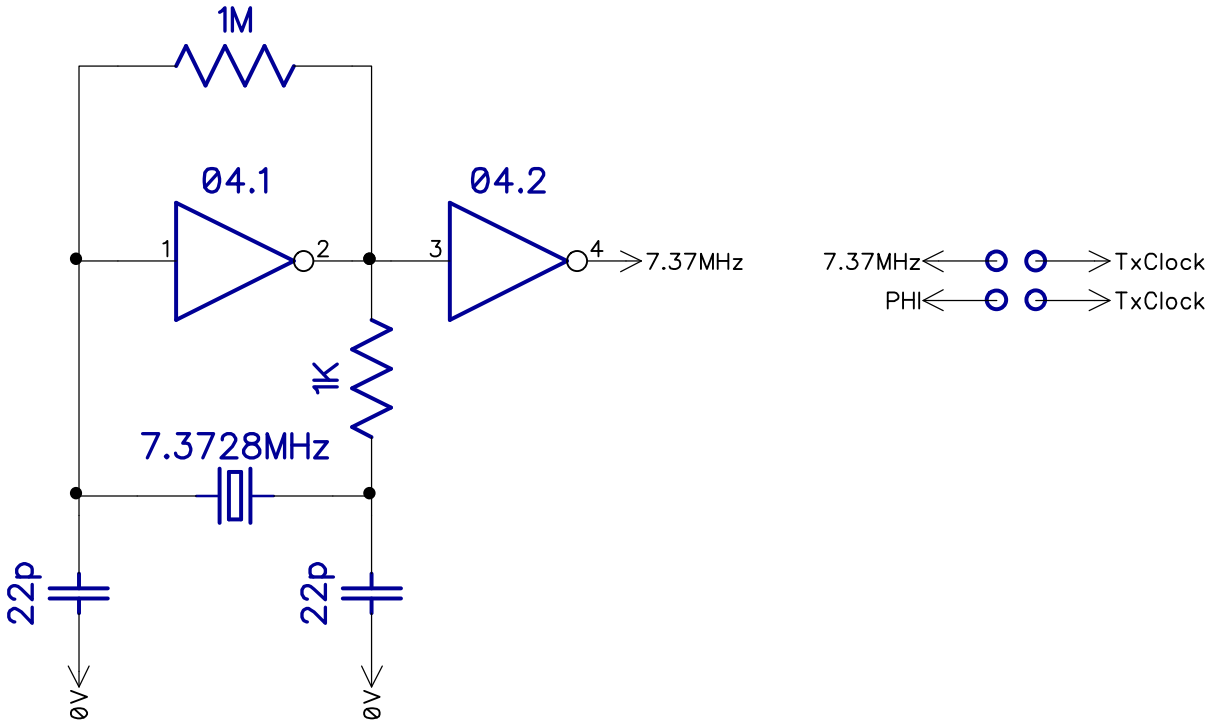
CLOCK CIRCUIT

SCHEMATIC

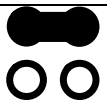
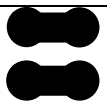


OVERVIEW

This is a fairly standard crystal oscillator circuit based around an inverter gate. The clock signal is buffered by the second gate.

The capacitor values shown will vary depending on the crystal used. The value is usually stated in the datasheet as load capacitance, and will be around 18-22pF.

The jumpers or hard wired links can be used to supply the UARTs Tx and Rx clock from the 7.3728MHz clock, or the bus clock, and also to feed the 7.3728MHz clock to both if there is no other clock source on the bus.

Jumper / Link	UART Clock	Bus Clock
	7.3728MHz	-
	Bus Clock	-
	7.3728MHz	7.3728MHz

68B50 UART

REGISTERS

Two of the four registers in the 68B50 are read only, and the other two are write only, so only two addresses are used. These will be mirrored over the range 0x80-0xBF, but 0x80 and 0x81 are suggested.

Address	Read	Write
0x80	Status	Control
0x81	Rx Data	Tx Data

STATUS REGISTER

The status register is read from address 0x80.

Bit	Function
0	Receive Data Register Full (RDRF)
1	Transmit Data Register Empty (TDRE)
2	Data Carrier Detect (DCD)
3	Clear To Send (CTS)
4	Framing Error (FE)
5	Receiver Overrun (OVRN)
6	Parity Error (PE)
7	Interrupt Request (IRQ)

CONTROL REGISTER

The control register is set by writing to address 0x80.

Bit	Function
0	Counter Divide Select 1 (CR0)
1	Counter Divide Select 2 (CR1)
2	Word Select 1 (CR2)
3	Word Select 2 (CR3)
4	Word Select 3 (CR4)
5	Transmit Control 1 (CR5)
6	Transmit Control 2 (CR6)
7	Receive Interrupt Enable (CR7)

TRANSMIT DATA

Transmit data is written to address 0x81. Poll TDRE to check then this has been set, or enable the interrupt.

RECEIVE DATA

Receive data is available by reading address 0x81. Poll RDRF to see if a new byte is available, or enable the interrupt.